Project Plan

Module Name	Algo Design/Sim Done	Verilog Done	Modelsim Done	FPGA Test Done
FFT	11/21	11/24	—	11/24
IFFT	11/21	11/24	—	11/24
Gain Curve Applier	11/21	11/22	11/22	11/24
Gain Curve Memories	—	11/24	—	11/24
VGA Output Controller	—	11/27	—	11/29
Gain Curve Displayer	11/21	11/27	—	11/29
Waveform Displayers	11/21	11/27	—	11/29
First UI (Incremental) FSM	—	11/29	11/30	12/1
First UI (Incremental) Calculator	11/21	11/29	11/30	12/1
Second UI (Mouse) PS/2 Module	—	12/1	—	12/5
Second UI Curve Builder	11/21	12/1	12/3	12/5